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(54) System for providing conversion of TDM-based frame relay data in a cross-connect matrix to and from ATM data

(57) A high density frame relay circuit within a digital cross-connect matrix converts TDM based DCS matrix data containing frame relay data to/from a DS3 ATM physical interface and provides adaption processing between the frame relay and ATM domains. The circuit is controlled by a DCS administrative subsystem and a simple network management protocol based network element manager.

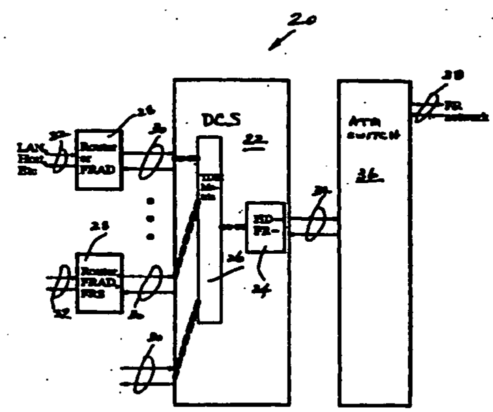

FIG. 1

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Description

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates to telecommunications systems, and more particularly to a system for converting TDM-based digital cross-connect system matrix data containing frame relay data to and from ATM data.

BACKGROUND OF THE INVENTION

[0002] Digital cross-connect systems (DCS) constitute switching/multiplex equipment that permit per-channel DS0 electronic cross-connection from one T1 transmission facilities to another, directly from the constituent DS1 signals. A basic multiplexing method used in telecommunications digital cross-connect systems is time division multiplexing (TDM). In TDM, a transmission facility is shared in time rather than frequency. In a TDM system, a frame is a sequence of time slots, each containing a sample from one of the channels served by the multiplex system. The frame is repeated at the sampling rate, and each channel occupies the same sequence position in successive frames. To permit higher levels of multiplexing concentration, a multi-level TDM digital signal hierarchy has been developed.

[0003] The DS1 level in the hierarchy corresponds to the 1.544Mbps TDM signal. The DS0 level refers to the individual time slot digital signals at channel rates of 64 kbps. Four DS1 signals comprise a DS2 level signal containing 96 DS0 channels. A DS3 level signal results from the digital multiplexing of seven DS2 signals. The DS designation refers to the signal level hierarchy and is independent of the type of carrier facility.

[0004] Frame relay is a high-speed switching technology utilized in a form of packet switching. The packets are in the form of "frames" which are variable in length. A frame relay network can accommodate data packets of various sizes associated with virtually any native data protocol.

[0005] Asynchronous transfer mode (ATM) is a high speed transmission technology utilizing a high bandwidth, low-delay, connection-oriented, packet-like switching and multiplexing technique. ATM allocates bandwidth on demand, making it suitable for high speed connection of voice, data, and video services.

[0006] In telecommunications systems, digital cross-connect systems are required to convert TDM based matrix data containing frame relay data to and from DS3 ATM data. Typically, equipment is separate from the cross-connect system that performs TDM-frame relay and frame-relay ATM conversion. Such equipment requires additional rack and bay locations from the digital cross-connect system as well as additional interfaces.

[0007] To improve the efficiency in telecommunications systems as well as to provide economical systems it is desirable to include additional functions within a digital cross-connect system. A need has thus arisen for a system to extract frame relay data from TDM data at a narrow band cross-connect switching matrix to perform conversion of the frame relay data to/from a DS3 ATM interface and perform adaption processing between the frame relay and ATM domains in a narrow band cross-connect system.

SUMMARY OF THE INVENTION

[0008] The present invention provides for a high density frame relay circuit pack to be installed in a subsystem of a digital cross-connect system. The frame relay circuit pack converts TDM based data containing frame relay data to/from a DS3 ATM physical interface and performs adaption processing between the frame relay and ATM domains. The frame relay circuit pack converts DS0 channelized and DS1 unchannelized frame relay traffic to DS3 ATM data in the outbound direction and converts DS3 ATM traffic to DS0 channelized or DS1 unchannelized frame relay data in the inbound direction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention and for further advantages thereof, reference is now made to the following Description of the Preferred Embodiments taken in conjunction with the accompanying Drawings in which:

FIG. 1 is a block diagram of the present telecommunications system including a digital cross-connect system and the present frame relay circuit;

FIG. 2 is a pictorial illustration of a telecommunications system showing the physical placement of equipment;

FIG. 3 is a block diagram of the present telecommunications system illustrating a redundant frame relay circuit;

FIG. 4 is a high level block diagram of the present frame relay circuit;

FIG. 5 is a detailed block diagram of the present frame relay circuit;

FIG. 6 is a block diagram of the present control processor block shown in FIG. 5;

FIG. 7 is a block diagram of the present frame engine block and physical layer interface block shown in FIG. 5; and

FIG. 8 is a block diagram of the matrix interface block shown in FIG. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] Referring to FIG. 1, a block diagram of the present telecommunications system, generally identi-

fied by the numeral 20 is illustrated. System 20 includes a digital cross-connect system (DCS) 22 and the present frame relay (FR) circuit 24. DCS 22 includes a TDM matrix 26. DCS 22 performs switching on time division multiplex traffic and provides access to frame relay 24 and asynchronous transfer mode services. DCS 22 may include, for example, a narrow band, tandem switch, or broad band cross-connect system.

[0011] TDM matrix 26 is connected to multiple routers, frame relay access devices (FRAD) 28 and frame relay service (FRS) 28 and communicates with these devices over T1 or E1 links 30. Router or FRAD 28 is interconnected to a local area network, or host over link 32, and converts internet protocol, and system network architecture data to and from frame relay data. Such conversion consists of adding data link connection identifiers (DLCI) address, frame check sequence, and other frame relay overhead. Links 30 carry DS1, E1 or DS3 with DS0, nXDS0, or DS1/E1 unchannelized frame relay TDM traffic.

[0012] DCS 22 grooms DS0s and increases utilization of DCS 22 TDM bandwidth, permanent virtual circuit throughput, and reduces port cost on frame relay switch 24. The output of frame relay circuit 24 represents DS3 ATM data transmitted over link 34 to an ATM relay switch 36. ATM relay switch 36 transmits ATM data over link 38 to a frame relay network including, for example, a DS1 trunk to/from another frame relay switch or to/from an end point frame relay access device router. An important aspect of the present invention is the use of frame relay circuit 24 installed within the subsystem of DCS 22.

[0013] The present frame relay circuit 24 is installed in a high density unit shelf of an equipment bay equipment rack. As illustrated in FIG. 2, DCS 22 includes an administrative bay 50, a matrix 26, bay 52, and a high density physical interface bay 54. Bay 50 houses an administrative shelf 56 and a timing shelf 58. Matrix subsystem bay 52 houses matrices A, and B, 60 and 62. High density relay circuits 24 are housed within bay 54 and includes, for example, up to 24 circuits 24 that may be installed within a unit shelf in a 1:1 sparing configuration. In the unprotected configuration 12, circuits 24 are installed, alternating one circuit 24 and one blank circuit pack for the twenty-four slots in a shelf. An extended back plane is used with matrix interface cables meeting above the card cage and network interface of the lower portion of the back plane.

[0014] FIG. 3 illustrates the architectural position of the present frame relay circuit 24 within DCS 22. DCS 22 includes an administrative subsystem 70 including synchronization circuit 72, microprocessor system 74, and AI system 76. Up to, for example, twelve pairs of circuits 24 per high density physical shelf are used in the 1:1 protected mode. Up to, for example, twelve single circuits 24 per shelf are used in the unprotected configuration. The high density unit shelf allows a mix of high density T1, HD-E1, HD-DS3 and frame relay circuits 24. The administrative/time subsystem 70 provides redundant timing buses for distribution to all circuits 24 within a shelf.

[0015] A serial link between microprocessor system 74 and each circuit 24 is used for system configuration and status uploads. Each circuit 24 is interfaced to both matrices 60 and 62. In the protected mode, each matrix 60 and 62 accepts inbound data from one side of circuit 24 pair. Each circuit 24 in the pair receives outbound data from both matrices 60 and 62. The matrix plane selection is performed under control of subsystem 70 or automatically by circuit 24 should the active matrix fail. Circuits 24 are connected to a high density interface 80 which outputs DS3 data. Circuits 24 include an Ethernet port which is connected to an Ethernet hub 82 which allows each circuit 24 to communicate to each other and connect to a high level element manager.

[0016] Referring now to FIG. 4 which is a high level block diagram of the present frame relay circuit 24. Physical layer interface 90 performs both DS3 line level interface and ATM transmission convergence sublayer functions. Physical layer interface 90 interfaces with a segmentation and re-assembly (SAR) block 92 via an 8-bit Utopia level 1 interface 94. Block 92 performs the upper portions of the ATM layer as well as the ATM adaptation layer. SAR 92 supports AAL 0, 3/4 and 5 cell formats as well as raw cell formats. A 32 bit peripheral component interconnect (PCI) bus 96 interfaces SAR 92 to a frame relay engine 98. Frame relay engine 98 performs data link layer operations through packetize/depacketize data and performs the interworking function between frame relay and ATM.

[0017] The output of frame relay engine 98 is applied to DCS interface 100 which converts serial data from/to the 16 bit DCS format, performs fault isolation, and selects the outbound redundant matrix plane to output to the network. Control processor 102 manages and configures all blocks interfaces with DCS 22 administration subsystem 70 (FIG. 3) and provides an Ethernet interface to the element manager. Timing block 104 selects the redundant timing input, generates board level clocks and performs fault isolation of the DCS 22 timing subsystem.

[0018] FIG. 5 illustrates a detailed block diagram of the present frame relay circuit 24. Frame engine 98, control processor 102, matrix interface 100, and physical layer interface 90 are illustrated, and will subsequently be described with respect to FIGs. 6-8. Physical layer interface 90 provides for DS3 line and path performance monitoring, ATM cell descrambling, vital/unassigned cell filtering, and includes four cell FIFO and sources Utopia 8 bit bus to SAR block 92. SAR block 92 reassembles convergence sublayer protocol data, writes convergence sublayer, protocol data unit (CS-PDUs) into the memory of frame relay engine 98. Additionally SAR 92 interrupts frame relay engine 98 when a complete CS-PDU is received, and interrupts frame relay engine 98 when operations administrative

and maintainance (OAM) cells are received.

[0019] Frame relay engine 98 converts CS/PDUs to frame relay packets. Frame relay packets may be formatted into DSO, nXDS0 or unchannelized DS1 for a total of 672 DS0 channels. Frame engine 98 further monitors frame relay data for performance gathering, performs conversion and writes converted data via PCI bus 96 to SAR block 92.

[0020] Matrix interface 100 converts serial frame engine 98 output to 16 bit DCS matrix format and generates frame sync based on system frame sync, for time slot alignment by HDCL controller 120. Matrix interface 100 further generates inbound DCS matrix overhead and redundant (matrix A, matrix B,) data is generated. On the outbound function, matrix interface 100 selects A or B outbound matrix plane under control processor direction. Matrix interface 100 further strips off DCS overhead and converts parallel PCM data to serial for processing by frame engine 98.

[0021] Referring simultaneously to FIGs. 5 and 6, control processor 102 functions to perform board configuration, DS3 line and path performance monitoring, diagnostics, and communication with layer 90 (FIG. 5), the companion circuit 24, simple network management protocol (SNMP) Ethernet LAN, and debug monitor. Firmware for circuit 24 is resident within control 102. Control block 102 includes a CPU 140 such as, for example, a model 68360 CPU manufactured and sold by Motorola, Inc. CPU 140 provides seven chip selects, six serial controllers, four timers, an interrupt controller, parallel ports and memory interface/control functions. In addition, an Ethernet controller 142 is used for SNMP management port.

[0022] The CPU 140 processor clock is created using an external crystal oscillator 144 and the phase lock loop within CPU 140. CPU 140 has built-in chip select generation which allows the memory map to be created under firmware control. This memory controller also generates DSACK and allows for programmable insertion of wait states. DRAM refresh is generated using the CAS before RAS method and a refresh.

[0023] CPU 140 includes four internal serial communication controllers, in which channel allocation includes Ethernet controller, SCL A asynchronous mode, SCL B, asynchronous mode, and HDUC comm asynchronous mode. Channel 1 is used for the Ethernet interface port. The Ethernet port is used for both debugging purposes as well as connectivity to a local area network for element management. The serial management controller is used as a debug port which has an RS-232 interface and is accessed via the back plane. CPU 140 includes two internal direct memory access controllers, one of which is connected to QSPAN 148 and cell processor 150 (FIG. 5).

[0024] Control block 102 includes two EPROM 152 which are connected to CS0 and only word wide access is permitted. EPROM 152 includes code for communications with administrative subsystem 70. Control block 102 further includes two DRAMS 154 which are refreshed using the CAS before RAS method. Control block 102 includes a control processor interface EPLD 156 which provides status and control registers for layer 90, protection switch relay control logic 158, SCL reset control logic, and SCL service and nonservice affecting alarm control. Control processor interface EPLD 156 controls a protection switch relay control 158 within layer 90 (FIG. 5). Control 158 arbitrates between circuit 24 card pairs to determine which card actually drives (transmits) the DS3 network line.

[0025] Control block 102 further includes ATM PHY 160 which functions as physical layer interface 90 (Fig. 4) and MI FPGA 162 which functions to perform outbound matrix parallel data to serial conversion.

[0026] Referring simultaneously to FIGs. 5 and 7, frame engine block 98 includes a processor 180 such as, for example, a MPC603e microprocessor manufactured and sold by Motorola, Inc. Frame engine 98 is connected to SAR 92, 6 HDLC controllers 182, and control block 102 via PCI bus 96. The PCI system memory, accessible by any PCI agent is also located within frame engine 98. The frame engine 98 PCI interface acts as both a master and a target. The PCI system memory accesses must vie with local frame engine bus accesses. In relation to the control processor block 102, frame engine 98 is viewed as a peripheral device accessed via the PCI bus 96. Firmware for frame engine 98 is resident within flash EEPROM 190 storage which is directly accessible only to frame engine 98. Frame engine 98 includes processor 180, PCI bridge memory controller 181, secondary (L2) cache module 184, system and PCI clock generator 186, synchronous DRAM memory banks 188, flash EEPROM memory banks 190, interrupt controller EPLD 192, and PCI arbitrator ELPD 194.

[0027] Frame engine interrupt controller 192 provides frame engine interrupt controller with miscellaneous physical layer and frame engine glue logic functions.

[0028] In relation to the control processor 140 (FIG. 5) within control block 102, frame relay processor 180 is simply viewed as a peripheral device which is accessible via the PCI bus 96. Control block 102 can reset the frame relay processor 180. Processor 180 includes one external level sensitive interrupt input, and in the system level context is intended to be a mechanism for SAR 92, HDLC controllers 182, and CP to request the attention of frame engine block 98. The interrupts from each of these devices are OR'd together in frame engine interface EPLD 192. Frame engine interface EPLD 192 provides the interrupt controller, PCI arbitrator 194, and miscellaneous physical layer and frame engine glue logic functions.

[0029] Referring now to FIGs. 5 and 8, matrix interface 100 converts DCS matrix data to/from frame engine PCI bus 96. In the outbound direction, the conversion process consists of reception and conversion of

A and B differential RS-422 data to single ended logic levels, selection of matrix plane for network transmission, parallel to serial conversion of selected matrix plane based on TDM location of DSO channels, grouping of each DSO channel into DS1 like serial links, and DSO channels which bear frame relay traffic are processed by HDLC receiver and burst across the PCI bus 96 to frame engine 98. In the inbound direction, matrix interface 100 functions to transmit data across PCI bus 96 from frame engine 98 to HDLC transmitter, serial to parallel conversion of serial DS1, channel Id is added to each of the parallel DSO channels, and inbound data is converted into A and B RS-422 differential copies and output to the matrix via the back plane.

[0030] Circuit 24 directly interfaces to DCS 22 and interfaces with redundant (A and B) inbound and outbound matrix and timing signals. Circuit 24 selects the best matrix plane (A or B) for the outbound path under firmware control. Firmware selects the best path based on path ID and parity performance. Circuit 24 interfaces with DSC 22 matrix via the back plane. RS-422 differential receivers and transmitters are used for the interface function. In the outbound direction, the receive termination is located on the back plane. In the inbound direction, the unused bits are not driven by RS-422 drivers to reduce power consumption; instead they are tied through resistors to produce a logic "0". RS-422 driver/receiver devices are used for this interface function.

[0031] Matrix interface 100 includes a matrix interface FPGA 210 which performs outbound matrix parallel data to serial conversion, selection of A or B outbound matrix plane, receives DS1 data lines from HDLC devices 120 and sources DS1 clock to the HDLC devices 120 in the inbound direction.
FPGA 210 also monitors the A and B timing busses for failures. Timing is provided in matrix interface 100 using PLL 214.

[0032] Referring again to FIG. 5, protection switch relay control within ATM layer 90 arbitrates circuit 24 protection pairs as to which circuit 24 is connected via relay 220 to the network DS3 line. This protection arrangement provides control over which circuit 24 is actively transmitting data to the network while allowing hardware to rapidly switch between active and standby circuits 24 in the event of a detected failure. Protection switch control hardware consists of relay 220 in the transmit DS3 paths and the control logic internal to control processor EPLD 156. Protection switch software uses the serial communication link between two circuits 24 to coordinate which of the cards is transmitting when both circuits 24 are fully functional. When both circuits 24 are fully functional, circuit path firmware controls which circuit 24 is actively transmitting to the network by a register within control processor EPLD 156 which produces the transmit relay enable to output close transmit relay 220.

[0033] Control processor EPLD 156 can automatically override the transmit enable control register bit setting if a failure condition is detected. For example, if a circuit 24 is currently active and its processor fails, control processor EPLD 156 will automatically open the transmit relay, and the control processor EPLD 156 on the companion circuit 24 will close the transmit relay. The inputs to this override logic include the local and companion card failure signals, the companion installed in the indicator and the card slot indicator. This logic provides an immediate automatic response to failure conditions.

[0034] Blocks 90, 98, 100, and 102 are all contained on a single printed circuit board or card comprising circuit 24 which is connected directly to DCS 22 including DCS 22 administrative subsystem 70. Circuit 24 represents an integrated function into DCS 22 but, instead of being a separate stand alone unit with its own independent control, circuit 24 operates internal to DCS 22. The present circuit 24 provides frame relay to ATM interworking for DSO channels which bear frame relay traffic.

[0035] Whereas the present invention has been described with respect to specific embodiments thereof, it will be understood that various changes and modifications will be suggested to one skilled in the art and it is intended to encompass such changes and modifications as fall within the scope of the appended claims.

Claims

1. A telecommunications system, comprising:

    a digital cross-connect matrix for receiving telecommunication traffic from any of a plurality of input ports and transmitting traffic to any of a plurality of output ports;
    a frame relay circuit connected to said digital cross-connect matrix for receiving frame relay traffic signals from said digital cross-connect matrix and for converting said frame relay traffic signals to asynchronous traffic mode signals for output to said plurality of output ports; and
    an administrative subsystem for controlling said digital cross-connect matrix and said frame relay circuit.

2. The telecommunications system of Claim 1 wherein said frame relay circuit includes:

    a matrix interface connected to said digital cross-connect matrix for converting serial data from said matrix and to said matrix in a matrix data format;
    a layer interface connected to said digital cross-connect matrix for converting said frame relay traffic signals to asnycnronous traffic mode signals;
    a frame engine circuit connect to said matrix

interface and said layer interface for packetizing and depacketizing data; and
a control circuit connected to said frame engine circuit, said layer interface circuit and said administrative subsystem.

3. The telecommunications system of Claim 2 wherein said matrix interface, layer interface, frame engine circuit and control circuit are disposed on a single printed circuit board.

4. The telecommunications system of Claim 2 wherein said matrix interface, layer interface, frame engine circuit and control circuit are interconnected via a PCI bus.

5. The telecommunications system of Claim 1 wherein said frame relay circuit includes a pair of frame relay circuits to provide redundancy for said digital cross-connect matrix.

6. The telecommunications system of Claim 1 wherein said digital cross-connect matrix comprises a narrow band cross-connect matrix.

7. The telecommunications system of Claim 1 wherein said digital cross-connect matrix comprises a broad band cross-connect matrix.

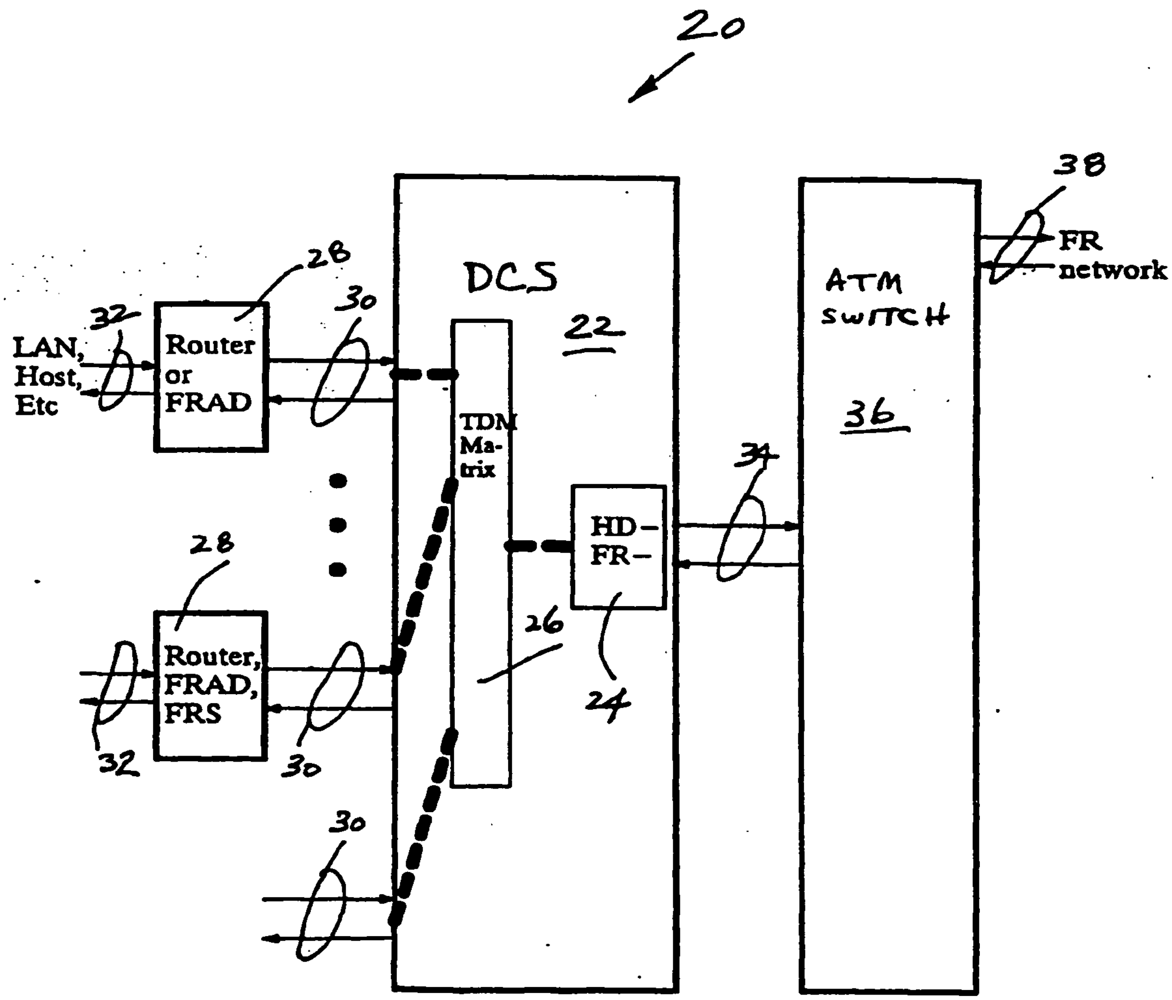
20
38
FR
network
28
DCS
ATM
SWITCH
32
30
22
LAN,
Host,
Etc
Router
or
FRAD
TDM
Ma-
trix
36
34
HD-
FR-
28
26
Router,
FRAD,
FRS
24
32
30
30

FIG. 1

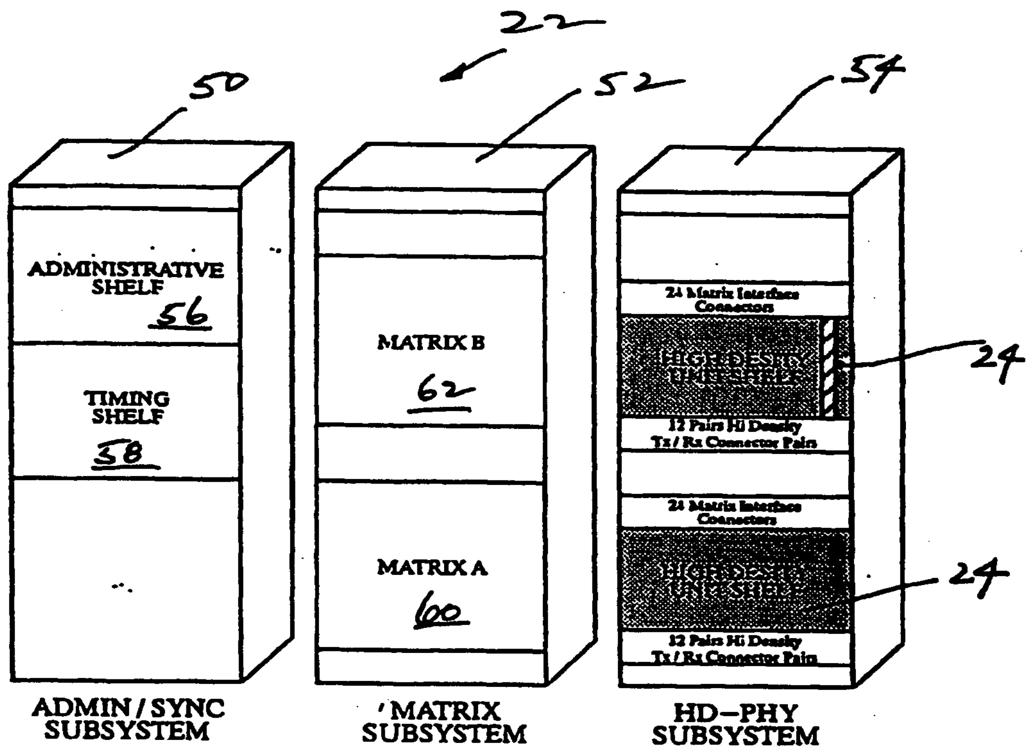
22
50
52
54
ADMINISTRATIVE SHELF
56
TIMING SHELF
58
MATRIX B
62
MATRIX A
60
24 Matrix Interface Connectors
HIGH DENSITY UNIT SHELF
12 Pairs Hi Density Tx / Rx Connector Pairs
24
ADMIN / SYNC SUBSYSTEM
MATRIX SUBSYSTEM
HD-PHY SUBSYSTEM

FIG. 2

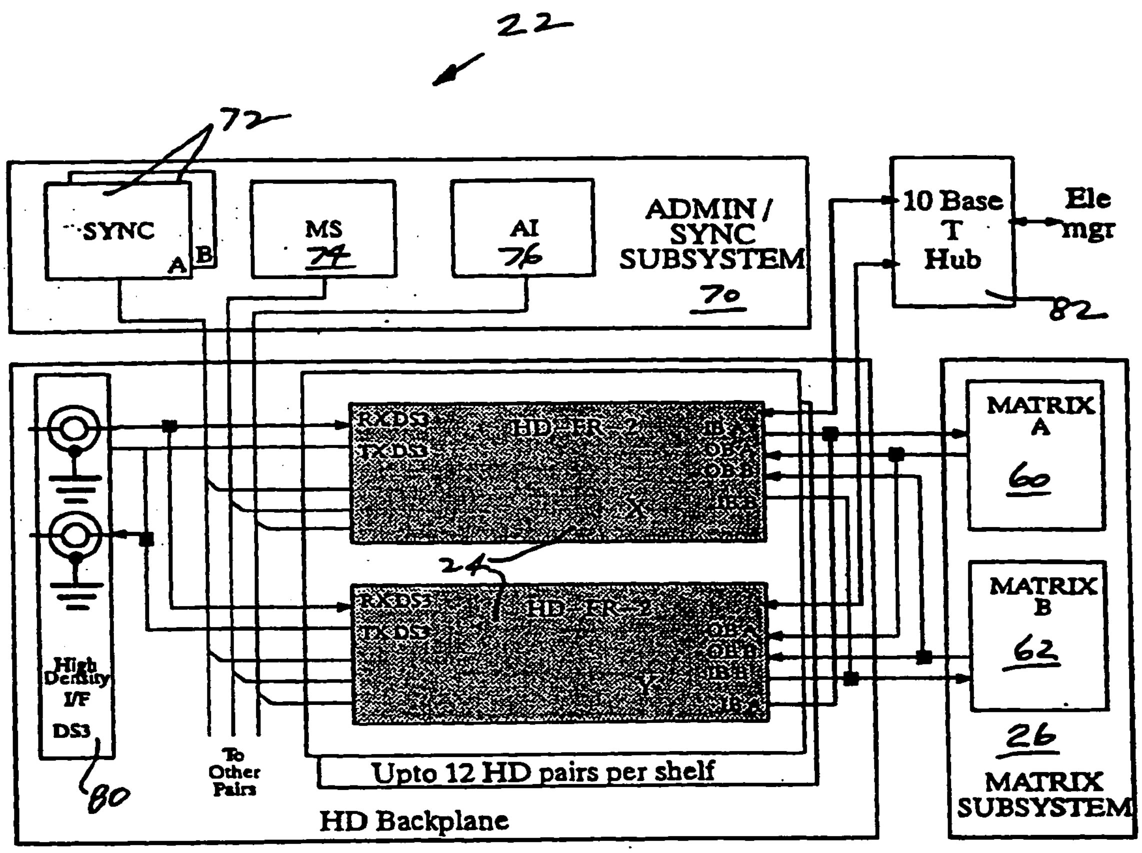
22
72
SYNC
A
B
MS
74
AI
76
ADMIN / SYNC SUBSYSTEM
70
10 Base T Hub
Ele mgr
82
RX DS3
TX DS3
HD - ER - 2
X
IB A
OB A
OB B
IB B
24
Y
MATRIX A
60
MATRIX B
62
26
MATRIX SUBSYSTEM
High Density I/F DS3
80
To Other Pairs
Upto 12 HD pairs per shelf
HD Backplane

FIG. 3

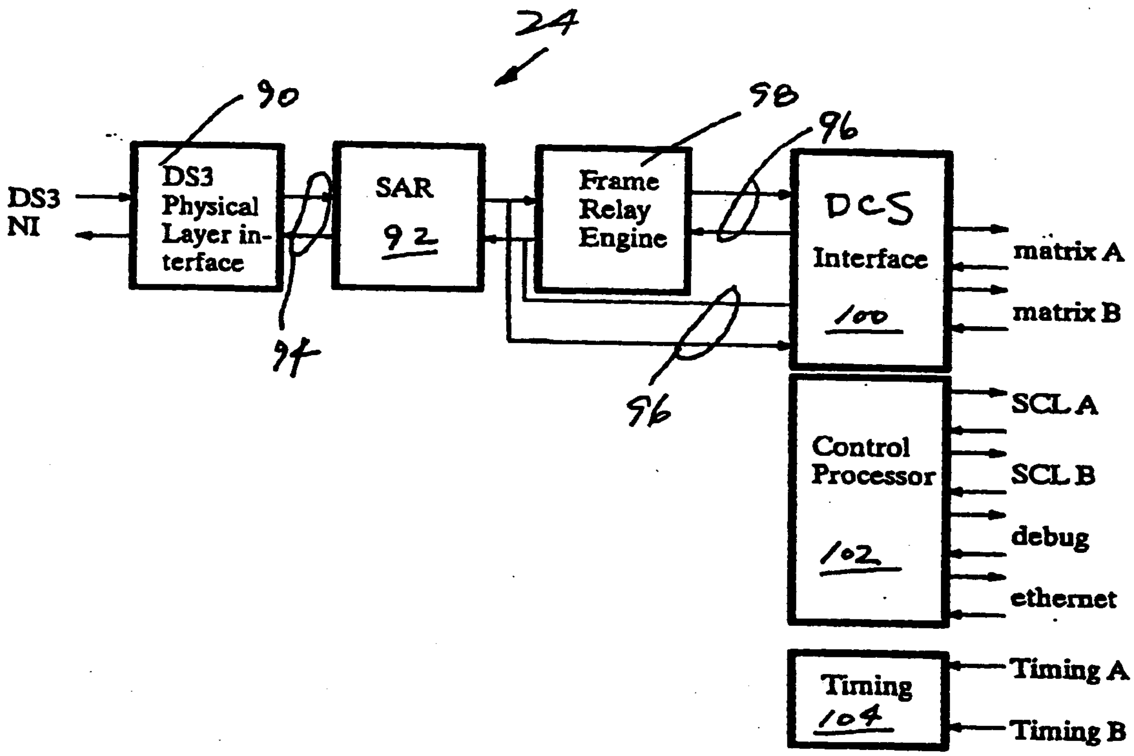
24
90
98
96
DS3
NI
DS3
Physical
Layer in-
terface
SAR
92
Frame
Relay
Engine
DCS
Interface
100
matrix A
matrix B
94
96
Control
Processor
102
SCL A
SCL B
debug
ethernet
Timing
104
Timing A
Timing B

FIG. 4

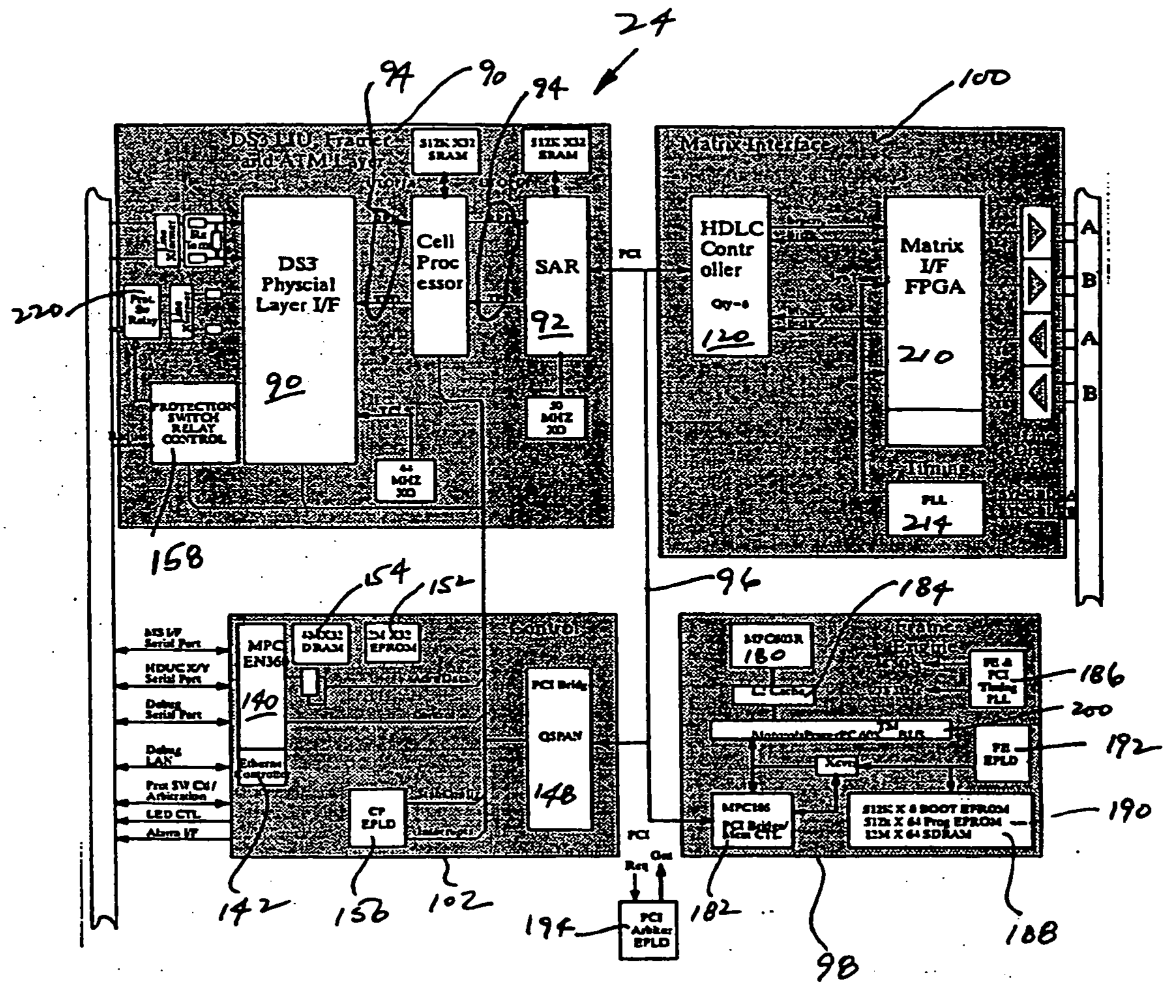
24
DS3 Physcial Layer I/F
90
Cell Proc essor
SAR
92
94
100
Matrix Interface
HDLC Contr oller
120
Matrix I/F FPGA
210
PLL
214
A
B
A
B
PCI
PROTECTION SWITCH RELAY CONTROL
158
220
MPC EN360
140
Ethernet Controller
142
PCI Bridge
QSPAN
148
CP EPLD
156
102
154
152
96
184
MPC603R
180
186
200
PB EPLD
192
MPC106 PCI Bridge/ Mem CTL
182
190
188
98
PCI Arbiter EPLD
194
Req
Gnt
DS3 I/F Serial Port
HDUC X/Y Serial Port
Debug Serial Port
Debug LAN
Prot SW Ctl/ Arbitration
LED CTL
Alarm I/F

FIG. 5

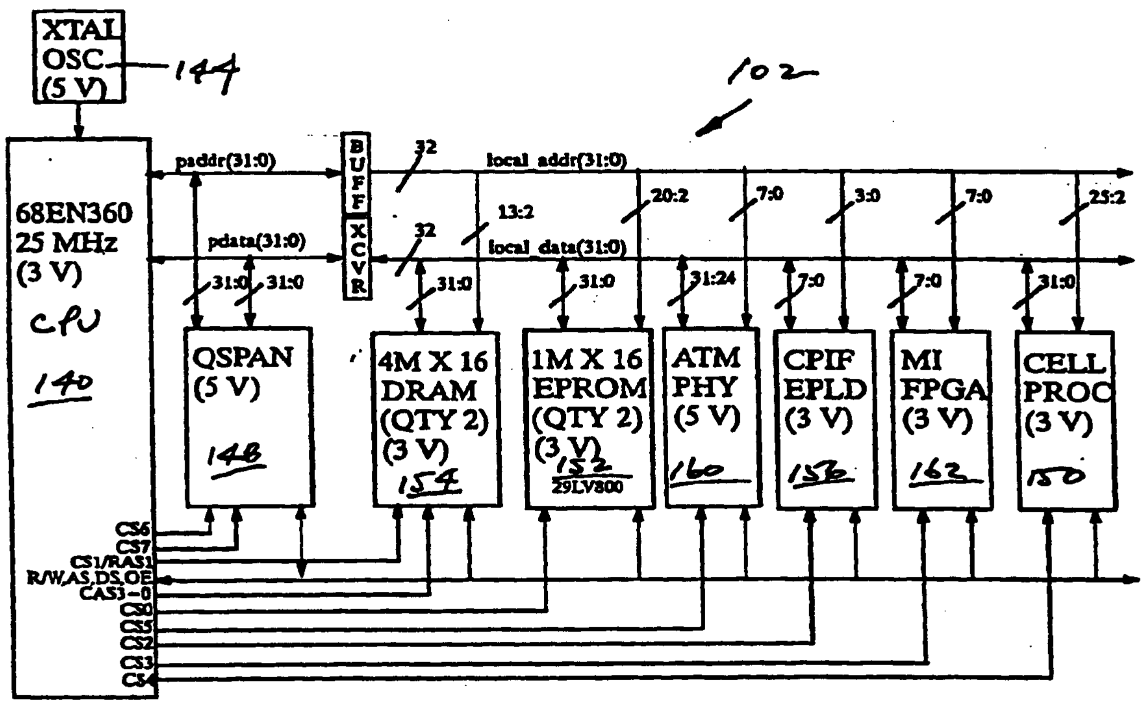
XTAL
OSC
(5 V)
144
102
68EN360
25 MHz
(3 V)
CPU
140
paddr(31:0)
pdata(31:0)
BUFF
XCVR
32
local addr(31:0)
local data(31:0)
13:2
20:2
7:0
3:0
7:0
25:2
31:0
31:24
QSPAN
(5 V)
148
4M X 16
DRAM
(QTY 2)
(3 V)
154
1M X 16
EPROM
(QTY 2)
(3 V)
152
29LV800
ATM
PHY
(5 V)
160
CPIF
EPLD
(3 V)
156
MI
FPGA
(3 V)
162
CELL
PROC
(3 V)
150
CS6
CS7
CS1/RAS1
R/W,AS,DS,OE
CAS3-0
CS0
CS5
CS2
CS3
CS4

FIG. 6

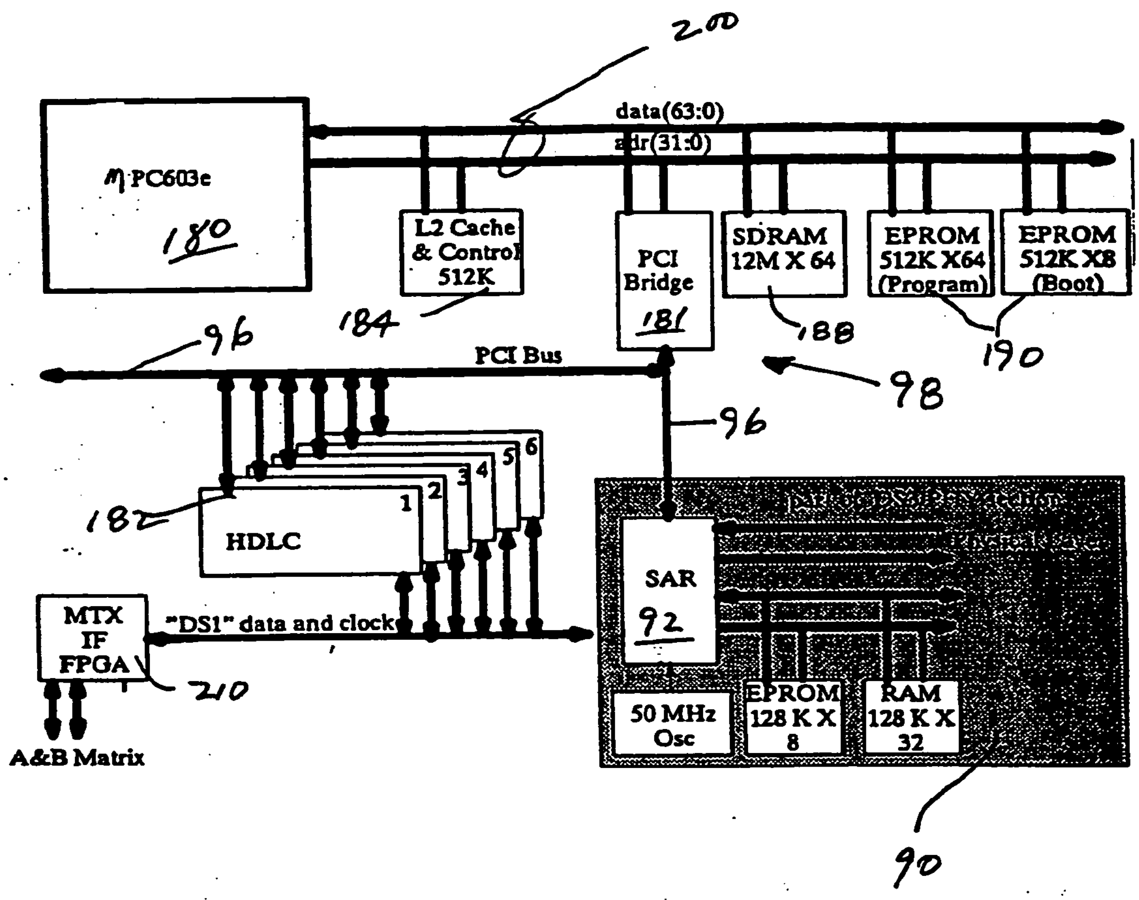
200
data(63:0)
adr(31:0)
PC603e
180
L2 Cache
& Control
512K
184
PCI
Bridge
181
SDRAM
12M X 64
188
EPROM
512K X64
(Program)
EPROM
512K X8
(Boot)
190
96
PCI Bus
98
96
182
HDLC
1
2
3
4
5
6
SAR
92
MTX
IF
FPGA
210
"DS1" data and clock
A&B Matrix
50 MHz
Osc
EPROM
128 K X
8
RAM
128 K X
32
90

FIG. 7

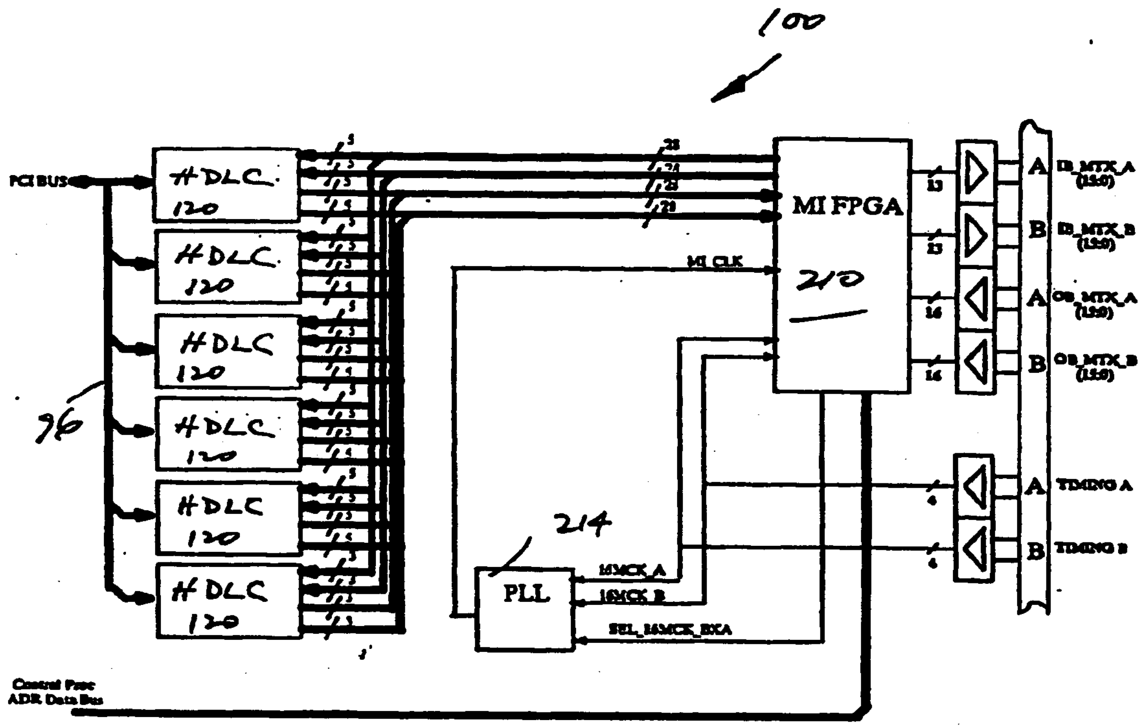
100
PCI BUS
HDLC 120
HDLC 120
HDLC 120
HDLC 120
HDLC 120
HDLC 120
96
MI FPGA
210
MI CLK
PLL
214
16MCK_A
16MCK_B
SEL_16MCK_EXA
Control Proc ADR Data Bus
IB_MTX_A (15:0)
IB_MTX_B (15:0)
OB_MTX_A (15:0)
OB_MTX_B (15:0)
TIMING A
TIMING B
A
B
A
B
A
B

FIG. 8